

A demodulation circuit for demodulating a multilevel digital modulation signal. Only an in-phase or quadrature component of the training signal generated in the demodulation circuit is used for equalization convergence. Tap coefficients of an equalizing training equalizer are updated by supplying either the in-phase or quadrature component so that the calculation amount can be reduced. When the equalization convergence is established, the obtained tap coefficients are rotated in phase and set to a data reproduction equalizer.